

Customer No.: 31561
Application No.: 10/708,178
Docket No.: 10929-US-PA

AMENDMENT

To the Claims:

Please amend the claims as follows:

Claims 1-8 (cancelled)

Claim 9. (currently amended) ~~The A driving stage as recited in claim 8 for an LCD driving circuit, the driving stage being a part of the LCD driving circuit in a cascade fashion, the driving stage comprising:~~

a clock input terminal, for receiving a clock signal having a first original level and a second original level;

a level shifter, coupled to the clock input terminal, for receiving the clock signal from the clock input terminal, for operating at a first target level and a second target level, and for amplifying the clock signal to a relay signal having a first relay level and a second relay level;

an output buffer, coupled to the level shifter, for receiving the relay signal from the level shifter, for operating at the first target level and the second target level, and for amplifying the relay signal to a target signal having the first target level and the second target level, wherein the first original level is higher than the second original level, the first target level is higher than the second target level, the first relay level is higher than

Customer No.: 31561
Application No.: 10/708,178
Docket No.: 10929-US-PA

the first original level but lower than the first target level, and the second relay level is lower than the second original level but higher than the second target level; and

a dynamic register, wherein the dynamic register is coupled to the clock input terminal for receiving the clock signal and determines whether the clock signal is provided to the level shifter according to a control signal, wherein the dynamic register comprises comprising:

a register output terminal, coupling to the level shifter;

a first control signal input circuit, receiving a previous stage driving signal from a previous driving stage and determining whether to conduct the clock signal to the register output terminal according to the previous stage driving signal; and

a second control signal input circuit, receiving a next stage driving signal from a next driving stage and determining whether to conduct the register output terminal the second target level according to the next stage driving signal.

Claim 10. (currently amended) The A driving stage as recited in claim 8 for an LCD driving circuit, the driving stage being a part of the LCD driving circuit in a cascade fashion, the driving stage comprising:

a clock input terminal, for receiving a clock signal having a first original level and a second original level;

a level shifter, coupled to the clock input terminal, for receiving the clock signal from the clock input terminal, for operating at a first target level and a second target level, and for amplifying the clock signal to a relay signal having a first relay level and a second

Customer No.: 31561
Application No.: 10/708,178
Docket No.: 10929-US-PA

relay level:

an output buffer, coupled to the level shifter, for receiving the relay signal from the level shifter, for operating at the first target level and the second target level, and for amplifying the relay signal to a target signal having the first target level and the second target level, wherein the first original level is higher than the second original level, the first target level is higher than the second target level, the first relay level is higher than the first original level but lower than the first target level, and the second relay level is lower than the second original level but higher than the second target level; and

a dynamic register, wherein the dynamic register is coupled to the clock input terminal for receiving the clock signal and determines whether the clock signal is provided to the level shifter according to a control signal, wherein the dynamic register comprises comprising:

a register output terminal, coupling to the level shifter;

a first control signal input circuit, receiving a previous stage driving signal from a previous driving stage and determining whether to conduct the clock signal to the register output terminal according to the previous stage driving signal; and

a second control signal input circuit, receiving the previous stage driving signal and output of the level shifter and determining whether to conduct the driving stage to the second target level thereby.

Claim 11. (original) The driving stage as recited in claim 10 further comprising:

a level chopper, couples the first target level to the register output terminal, and

Customer No.: 31561
Application No.: 10/708,178
Docket No.: 10929-US-PA

determines whether to conduct the register output terminal to the first target level according to the previous stage driving signal.

Claim 12. (original) The driving stage as recited in claim 11, wherein the level chopper comprises p-type thin film transistor.